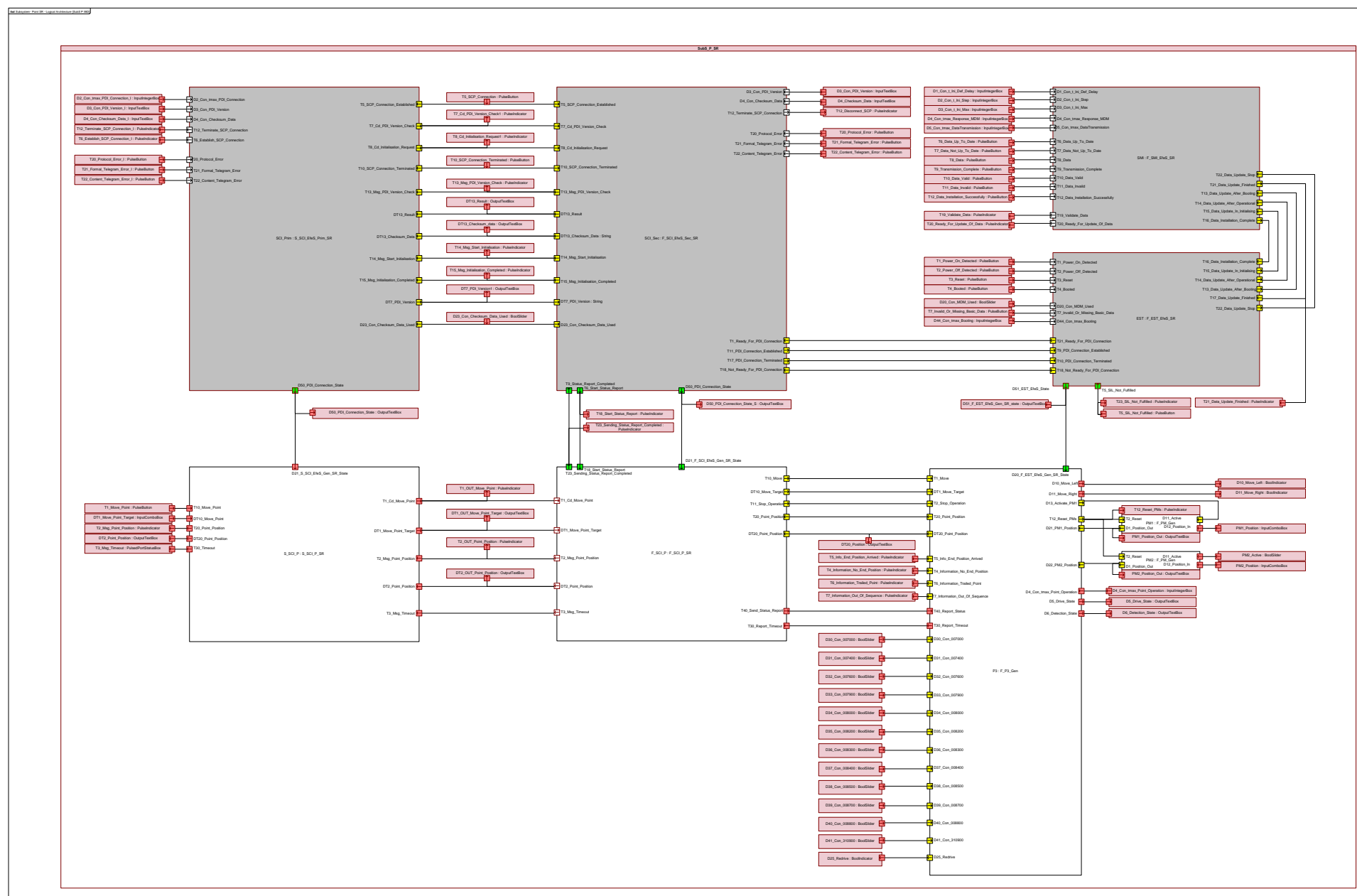
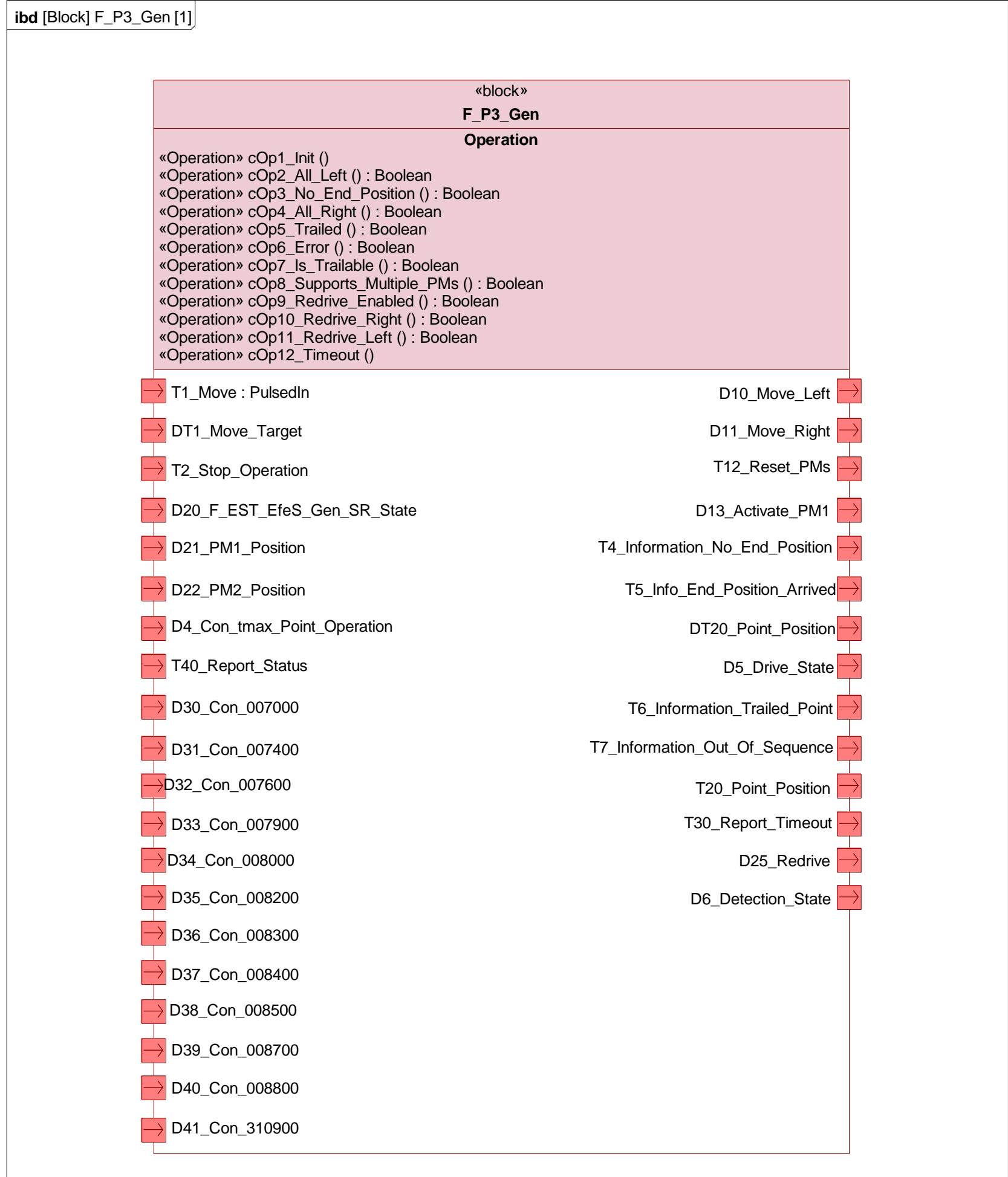
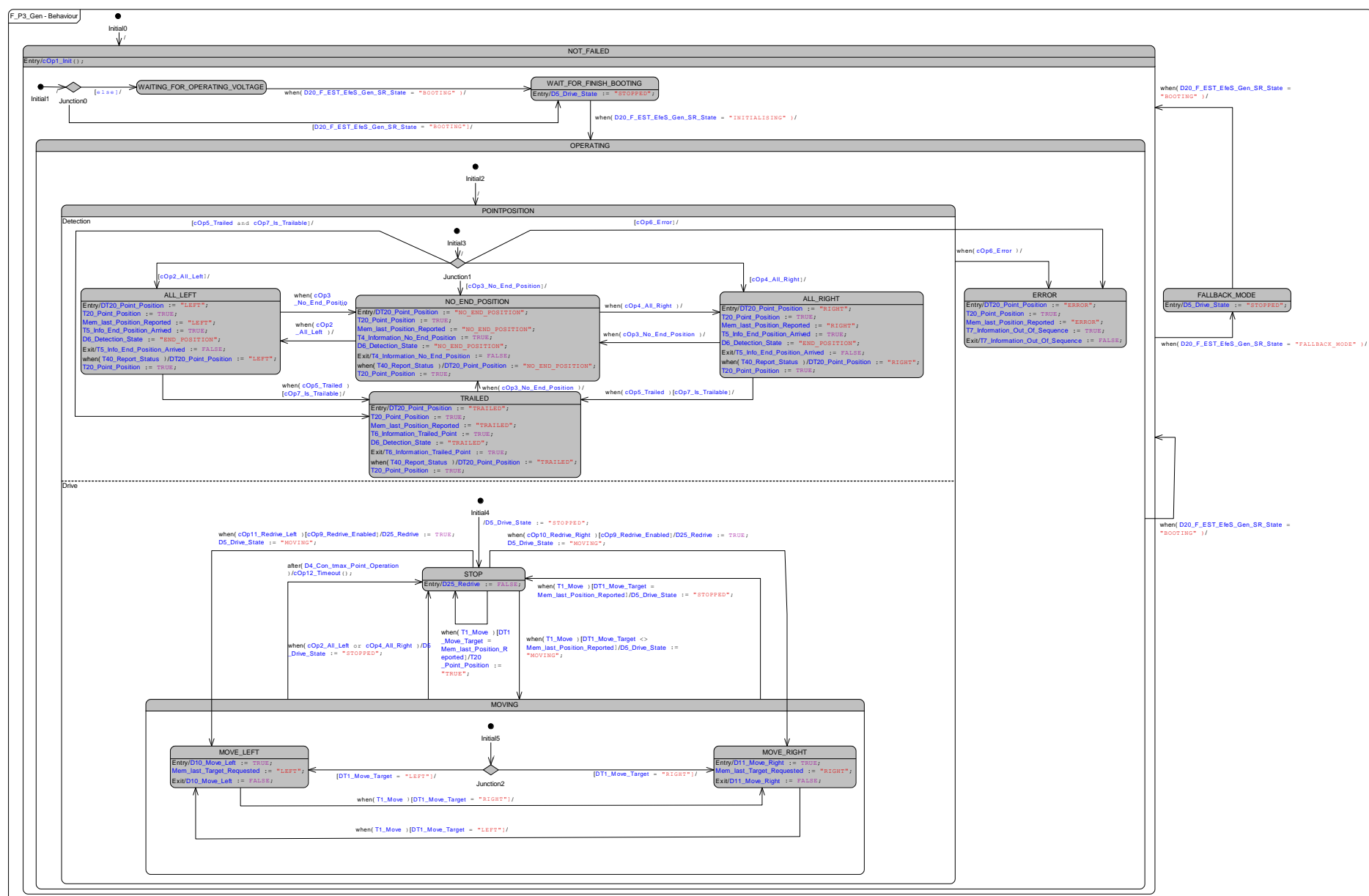


SUP_P_SR Logical Architecture



F_P3_Gen





F_PM_Gen

